AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Cancel Claims 1-8 without prejudice.

9. (Previously amended) An electronic design automation system for verifying a user design, comprising:

a computing system including a central processing unit and memory for modeling the user design in software;

an internal bus system coupled to the computing system;

reconfigurable hardware logic coupled to the internal bus system and for modeling at least a portion of the user design in hardware;

control logic coupled to the internal bus system for controlling the delivery of data between the reconfigurable hardware logic and the computing system; and

VCD on-demand logic for recording at least a portion of a selected simulation session range and dumping state information from the hardware model into a VCD file for a selected simulation target range, wherein the simulation target range is within the simulation session range, and wherein said value change dump (VCD) file is dedicated to the state information in the selected simulation target range and is exclusive of state information outside said selected simulation target range.

10. (Previously presented) The electronic design automation system of claim 9, wherein the VCD on-demand logic further comprises:

first range selection logic for selecting a simulation session range which begins at a simulation time t0 and ends at a simulation time t3;

second range selection logic for selecting a simulation target range which begins at a simulation time t1 and ends at a simulation time t2, wherein the simulation time t1 is greater than or equal to simulation time t0 and simulation time t2 is less than or equal to simulation time t3;

dump logic for generating a VCD file of the hardware-modeled design for the

selected simulation target range; and

access logic for accessing the VCD file directly from simulation time t1 to debug the user design.

11. (Previously presented) The electronic design automation system of claim 10, wherein the VCD on-demand logic further comprises:

test bench process for providing primary inputs to the hardware-modeled design for evaluation; and

recording logic in the computing system for recording data associated with at least one parameter in the simulation session range.

12. (Previously presented) The electronic design automation system of claim 11, wherein the VCD on-demand logic further comprises:

process logic in the computing system for loading the recorded data associated with the at least one parameter; and

evaluation logic in the reconfigurable hardware logic for evaluating in the hardware-modeled design the primary inputs from simulation time t0 to simulation time t2.

13. (Previously presented) The electronic design automation system of claim 12, wherein the dump logic dumps the evaluated results from the hardware-modeled design based on the primary inputs during the simulation target range into the VCD file.

14. (Previously presented) The electronic design automation system of claim 13, wherein the recording logic further comprises:

compression logic for compressing the primary inputs;

write logic for writing the compressed primary inputs and state information from the hardware model at simulation time t0.

15. (Previously presented) The electronic design automation system of claim 14, wherein the process logic further comprises:

decompression logic for decompressing the compressed primary inputs; and

data transfer logic for delivering the decompressed primary inputs to the hardware-modeled design for evaluation.

16. (Previously presented) The electronic design automation system of claim 13,

wherein the recording logic further comprises:

write logic for writing the primary inputs and state information from the hardware model at simulation time t0.

17. (Previously presented) The electronic design automation system of claim 9, further comprising:

state save logic for saving state information of the hardware-modeled design at simulation time t0 in a first file and saving state information of the hardware-modeled design at simulation time t3 in a second file.

Cancel Claims 18-22 without prejudice.